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(71) Applicant: Omnivision Technologies Inc.
Sunnyvale, California 94086 (US)

(72) Inventors:
- Zhao, Tiemin
Palo Alto, CA 94306 (US)
- He, Xinping
San Jose, CA 95148 (US)
- Chen, Datong
Fremont, CA 94555 (US)

(74) Representative: Hackney, Nigel John et al
Mewburn Ellis,
York House,
23 Kingsway
London WC2B 6HP (GB)

(54) Floating region photodiode for a CMOS image sensor

(57) A photodiode with an optimized floating P+ region for a CMOS image sensor. The photodiode is constructed with a P+/Nwell/Psub structure. The Nwell/Psub junction of the photodiode acts as a deep junction photodiode which offers high sensitivity. The P+ floating region passivates the silicon surface to reduce dark currents. Unlike a traditional pinned photodiode structure, the P+ region in the present invention is not connected to the Pwell or Psub regions, thus making the P+ region floating. This avoids the addition of extra capacitance to the cell. The photodiode may be included as part of an active pixel sensor cell, the layout of which is fully compatible with the standard CMOS fabrication process. This type of active pixel sensor cell includes the photodiode, and may be configured with a three transistor configuration for reading out the photodiode signals. Examples of other configurations that the photodiode can be used with include two transistors, four transistors, log scale, as well as its ability to be used in a passive pixel implementation. Also, an additional optional N type layer can be introduced in between the P+ region and Nwell to fine tune the junction profile for special applications. In addition, the field oxide region may be made to extend over the photodiode, so as to reduce the exposure of the diode area to the field oxide region edge, which can be a source of dark current due to the high electric fields and mechanical stresses.

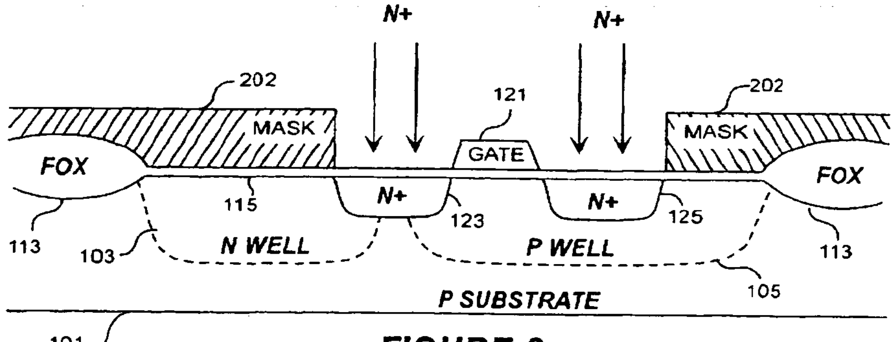

FIGURE 6

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Description

[0001] The present invention relates to image sensing devices, and more particularly, to a pixel sensor cell.

[0002] Integrated circuit technology has revolutionized various fields, including computers, control systems, telecommunications, and imaging. In the field of imaging, the charge coupled device (CCD) has been made popular by its manufacturing and performance characteristics, including its relatively low cost and small size. Nevertheless, the solid state CCD integrated circuits needed for imaging are relatively difficult to manufacture, and therefore are expensive. In addition, because of the differing processes involved in the manufacture of the CCD integrated circuits relative to MOS integrated circuits, the signal processing portion of the imaging sensor has typically been located on a separate integrated chip. Thus, a CCD imaging device includes at least two integrated circuits: one for the CCD sensor and one for the signal processing logic.

[0003] Another class of image sensors are the active pixel sensors. As noted in U.S. Patent No. 5,625,210 to Lee et al. ("the '210 patent), an active pixel sensor refers to an electronic image sensor with active devices, such as transistors, that are associated with each pixel. The active pixel sensor has the advantage of being able to incorporate both signal processing and sensing circuitry within the same integrated circuit. Conventional active pixel sensors typically employ polysilicon photocapacitors or photodiodes as the image sensing elements.

[0004] The most popular active pixel sensor structure consists of three transistors and a N+/Pwell photodiode, which is a structure that is compatible with the standard CMOS fabrication process. Examples of other structures are shown in U.S. Patent No. 5,587,596 (showing a one transistor cell), U.S. Patent No. 5,926,214 (showing an N-transistor cell), and U.S. Patent No. 5,933,190 (showing a log scale sensor). In such sensors, desirable characteristics include the ability for the device to have high sensitivity, combined with a low dark current (i.e., the current that is output from the sensor in a dark environment). In the design of active pixel sensors, it is known that for the same sensor size, a deeper junction photodiode will have a higher sensitivity than that of a shallow junction (such as in a typical N+/Pwell). However, the production of such devices usually requires modifications to the standard CMOS fabrication process, and in addition may increase dark current due to larger effective junction areas (when considered from a three-dimensional perspective).

[0005] Thus, two of the presently available alternatives are to either use the standard three-transistor plus N+/Pwell photodiode structure that can be formed with the standard CMOS fabrication process, or else abandon the standard CMOS fabrication process in favor of designs that are intended to improve the sensitivity and dark current characteristics. One active pixel sensor design that is not fabricated using the standard CMOS fabrication process is the pinned photodiode, as taught in the '210 patent.

[0006] The pinned photodiode has gained favor for its ability to have good color response for blue light, as well as advantages in dark current density and image lag. Reduction in dark current is accomplished by pinning the diode surface potential to the Pwell or Psubstrate (GND) through a P+ region. While the '210 patent provides a method for using a pinned photodiode and an active pixel sensor, the design taught suffers from the drawback of manufacturing complexity. In particular, as seen in the diagrams of the '210 patent, the manufacture of such an apparatus requires multiple masking and photolithography steps.

[0007] An improvement over the device taught in the '210 patent is shown in U.S. Patent No. 5,880,495 to Chen (the'495 patent), which is hereby incorporated by reference. The '495 patent teaches an active pixel pinned photodiode structure that can be made with one less mask than the structure taught in the '210 patent. This is accomplished by removing the need for an N- channel underneath the transfer gate as shown in the '210 patent. Instead, a highly doped N+ well (a "transfer well") adjacent to the transfer gate is formed that aids in the transfer of charge (the photo signal) from the pinned photodiode to the output circuitry. In addition, the masking steps shown in the '210 patent to form the lightly doped N- channel must be precisely aligned to be underneath the transfer gate. In contrast, the alignment of the mask in the '495 device is relatively robust to misalignment.

[0008] Even with the improved structure taught in the '495 patent, the pinned photodiode configuration still has certain drawbacks. For example, in a pinned photodiode structure there are four transistors, so the fill factor is smaller for the same area, which results in less sensitivity. In addition, the fabrication process for such a configuration requires significant modification from the standard CMOS fabrication process, due to the buried channel TG transistor. As also noted with reference to the '210 patent, the pinned photodiode configuration may cause image lag due to the incomplete transfer of charge from the diode to the floating node, if the junction profile is not perfectly optimized for the charge transfer.

[0009] Thus, what is needed, is a pixel photodiode structure that can be formed utilizing the standard CMOS process, while having a high sensitivity and low dark current.

[0010] A pixel sensor for use in an imaging array and formed in a semiconductor substrate having a first conductivity-type is disclosed. In accordance with one aspect of the invention, the pixel sensor includes a photodiode which is constructed with a P+/Nwell/Psub structure.

[0011] The Nwell/Psub junction acts as a deep junction photodiode which offers high sensitivity. The P+ region passivates the silicon surface to reduce dark current. Unlike a pinned photodiode structure, the P+ re-

gion in the present invention is not connected to the Pwell or Psub layers, thus making the P+ region floating. This avoids the addition of extra capacitance to the cell. When a contact is made to the diode, the performance may be improved by making sure that the P+ in the contact area is blocked to ensure that it is floating, while also making sure that the N+ is present to ensure good contact to the Nwell.

[0012] In accordance with another aspect of the invention, the photodiode is implemented as an active pixel sensor cell, then entire layout of which is compatible with the standard CMOS fabrication process. In addition, this active pixel sensor cell device can be formed utilizing the standard three transistor cell, as opposed to the four transistor cell required for the pinned photodiodes. Alternatively, other configurations may also be used with the photodiode, such as a passive pixel, a two transistor, a four transistor, or a log scale cell.

[0013] In accordance with another aspect of the invention, the three transistor active pixel sensor cell includes a reset transistor formed in a semiconductor substrate next to the photodiode, as well as a buffer transistor and a row select transistor. To form the reset transistor, a Pwell is formed in a semiconductor substrate next to the Nwell of the photodiode. Thereafter, a gate is formed over the Pwell, and the source and drain N+ regions are also formed. The drain N+ region is formed over the Pwell, whereas the source N+ region is formed over part of the junction between the Nwell and the Pwell. A field oxide isolation region (e.g., LOCOS isolation) is formed on either side of the Nwell and the Pwell.

[0014] In accordance with another aspect of the invention, an additional N type region can be introduced in between the P+ region and Nwell to fine-tune the junction profile for special applications.

[0015] In accordance with another aspect of the invention, another variation to the structure is to have the P+/Nwell/Psub photodiode all under the field oxide isolation region. This reduces the exposure of the diode area to the field oxide isolation region edge, which can be a source of dark current due to the high electric fields and mechanical stresses.

Brief Description of the Drawings

[0016] The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same become better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIGURE 1 is a Psubstrate with a first mask to begin the formation of a pixel sensor according to the present invention;
FIGURE 2 shows the formation of an Nwell in the Psubstrate;
FIGURE 3 shows the formation of a Pwell in the Psubstrate;
FIGURE 4 shows the addition of the field oxide regions and a poly layer;
FIGURE 5 shows the formation of a gate from the poly layer;
FIGURE 6 shows the formation of N+ regions on either side of the gate;
FIGURE 7 shows the formation of a floating P+ region as part of the photodiode;
FIGURE 8 shows a partial circuit diagram illustrating the connections of a completed active pixel sensor device with a three transistor structure;
FIGURE 9 shows an alternate embodiment with an additional N type region; and
FIGURE 10 shows another alternate embodiment in which the photodiode is located under the field oxide region edge.

[0017] The present invention is an improvement to the active pixel sensors taught in the '210 and '495 patents. Much of the description of the circuitry of an active pixel sensor is recited in the '210 patent and the cited references in the '210 patent. Those designs are considered to be instructive as to the basic design and operation of active pixel sensors.

[0018] The present invention is an active pixel sensor that can be formed with the standard CMOS fabrication process, while also having the desirable characteristics of high sensitivity combined with a low dark current. The dark current is reduced by utilizing a P+ region that passivates the silicon surface. Unlike the pinned photodiode structures, the P+ region in the present invention is not connected to the Pwell or Psub regions, thus making it floating. The floating P+ region avoids the addition of extra capacitance to the cell.

[0019] As previously noted, the device of the present invention is formed using the standard CMOS fabrication process. In the description below, the preferred dopant for N type implant is Phosphorus, while the preferred dopant for a P type implant is Boron. The standard CMOS fabrication process may start with a P type semiconductor substrate, as illustrated in FIGURE 1. As illustrated in FIGURE 1, a P type semiconductor substrate 101 is initially covered with a photolithography mask 201. The photolithography mask 201 leaves a portion of the Psubstrate 101 exposed, so that it may receive a first N type ion implant, as illustrated with respect to FIGURE 2.

[0020] As illustrated in FIGURE 2, a first N type ion implant is performed to implant a deep Nwell 103. As will be described in more detail below, the Nwell 103 that is implanted in the Psubstrate 101 will also include an additional P+ region, so as to form a P+/Nwell/Psub photodiode. In accordance with the present invention, the Nwell 103 is formed fairly deep in the substrate, so as to increase the sensitivity of the photodiode. The increase in sensitivity is achieved because the deep implant yields substantial increases in the photo response,

due to an increase collection path for the instant photogenerated carriers.

[0021] As illustrated in FIGURE 3, a photolithography mask 202 is deposited onto a portion of the Psubstrate. Thereafter, a P type ion implant is performed to create a deep Pwell 105. As will be described in more detail below, the Pwell is used in part for the formation of a reset transistor, as well as buffer transistor 151 and row select transistor 153.

[0022] As illustrated in FIGURE 4, field oxide regions 113 are formed in the substrate 101 using any suitable conventional semiconductor processing method, such as LOCOS. The field oxide regions 113 define an active area in which the photodiode is formed. Also formed on top of the substrate 101 between the field oxide regions 113 is an isolation oxide 115. The isolation oxide 115 is also referred to as a gate oxide and is preferably formed from silicon dioxide. The method that is used to form the silicon dioxide isolation oxide layer 115 can be one of any well known techniques, including the thermal oxidation of silicon. As also shown in FIGURE 4, a layer of polysilicon 117 is deposited over the substrate 101. The polysilicon may be deposited using any conventional technique, such as low pressure chemical vapor deposition (LPCVD).

[0023] As illustrated in FIGURE 5, the polysilicon layer 117 is patterned and etched using conventional photolithography and masking techniques to form a control gate 121. As described below, this will be the gate 121 for the reset transistor.

[0024] As illustrated in FIGURE 6, a photolithography mask 203 is deposited. The mask 203 is formed using conventional lithography techniques. Thereafter, high concentration doping is used to form N+ regions using the mask 203 as an implementation mask. The implementation of the high concentration doping is performed using known techniques in the prior art and conventional dopants. This forms an N+ region 123 and an N+ region 125. Note that the N+ region 123 is formed at the border between the Nwell 103 and the Pwell 105. As will be described in more detail below, the N+ regions 123 and 125 will be used as the source and drain of the reset transistor.

[0025] As illustrated in FIGURE 7, a photolithography mask 204 is deposited, leaving exposed a region between one of the field oxide regions 113 and the N+ region 123. Thereafter, high concentration doping is used to form a P+ region using the mask 204 as an implementation mask. This forms the P+ region 131, which is the previously described floating P+ region of the photodiode, which passivates the silicon surface to reduce dark currents. The P+ region formation can be the same as the PMOS source/drain implant that is done as part of the standard CMOS process. Unlike the pinned photodiode structure, the P+ region 131 of the present invention is not connected to the Psubstrate 101 or the Pwell 105, thus making it floating. Therefore, the P+ region 131 does not add extra capacitance to the cell. It is noted that when a contact is made to the photodiode, the P+ region in the contact area should be blocked to ensure that it is floating, and N+ should be present to ensure good contact to the Nwell 103.

[0026] As further described in the '210 patent and as seen in FIGURE 8, the N+ region 123 is connected to output circuitry. The output circuitry includes a buffer transistor 151, in addition to a row select transistor 153. The N+ region 123 is coupled to the gate of the buffer transistor 151, while the drain of the buffer transistor 151 is coupled to a fixed voltage such as V_{DD}. The source of the transistor 151 is coupled to the drain of the row select transistor 153, while the source of the transistor 153 provides the output of the processing circuitry. The gate of the row select transistor 153 receives a row select signal RS.

[0027] As also illustrated in FIGURE 8, the N+ region 125 is connected to a fixed voltage such as the supply voltage V_{DD}. The reset gate 121 is periodically activated by a reset signal. When the reset signal is "on," the channel under the reset gate 121 is made conducting, and current is able to flow through the transistor so as to reset the photodiode.

[0028] As illustrated, the present invention provides an active pixel photodiode structure that can be formed with the standard CMOS process. In addition, the device of FIGURE 8 is formed with only three transistors, as compared to the four transistors required for the previously described pinned photodiodes. As a result, for a given fabrication area, the present device can devote more area to photosensing rather than the processing circuitry. In addition, this avoids the image lag that can sometimes result in pinned photodiodes due to an incomplete transfer of charge from the diode to the floating node, in cases when the junction profile is not perfectly optimized for the charge transfer.

[0029] The described structure of the present invention provides for a deep junction photodiode, as seen in the deep Nwell/Psub junction (as seen between the Nwell 103 and the Psubstrate 101), thereby providing for high sensitivity of the device. In addition, dark current is reduced in that the P+ region 131 passivates the silicon surface. As noted above, the P+ region 131 is not connected to the Pwell 105 or the Psub 101, thus making the P+ region 131 floating. Because the P+ region 131 is floating, it does not add extra capacitance to the cell.

[0030] FIGURE 9 shows an alternate embodiment of the invention. As illustrated in FIGURE 9, an additional N type region 141 has been introduced in between the P+ region 131 and the Nwell 103. This additional N type region 141 is added to fine-tune the junction profile for special applications.

[0031] FIGURE 10 illustrates another alternate embodiment. As illustrated in FIGURE 10, the field oxide region 113 is now located over the P+/Nwell/Psub photodiode. By having this photodiode under the field oxide insulation 113, the exposure of the diode area to the field

oxide edge is reduced. The exposure of the diode area to the field oxide edge can be a source of dark current due to the high electric fields and mechanical stresses experienced in this region.

[0032] While the preferred embodiment of the invention has been illustrated and described, it will be appreciated that various changes can be made therein without departing from the spirit and scope of the invention. For example, while the formation of the active pixel sensor illustrated in FIGURES 2 and 3 has generally shown the Nwell 103 being formed before the Pwell 105, these processes could be performed in the reverse order. In addition, while the formation of the field oxide regions 113 in FIGURE 4 was generally illustrated as being formed after the Nwell 103 and Pwell 105, the Nwell and/or Pwell could be formed after the formation of the field oxide regions 113. While the N+ regions 123 and 125 of FIGURE 6 were generally shown as being formed before the P+ region 131 of FIGURE 7, these processes could be performed in reverse order. In addition, the optional N type region 141 of FIGURE 9 can be formed either before or after the N+ regions 123 and 125 and the P+ region 131. In addition, the optional N region 141 of FIGURE 9 could be formed between the N+ regions 123 and 125 and the P+ region 131, or between the P+ region 131 and the N+ regions 123 and 125. It is also understood where the device has generally been shown using different types of P or N type materials, the types of materials could be switched to produce similar results. For example, rather than the P+/Nwell/Psub photodiode that was formed with respect to the P+ layer 131, Nwell 103, and Psubstrate 101, the alternate types of materials could be used to form a N+/Pwell/Nsub photodiode.

[0033] In addition, the above-described photodiode could also be used in other applications. For example, rather than an active pixel sensor, the photodiode could be implemented in a passive pixel sensor. Also, rather than being implemented in a three transistor active pixel sensor, other styles of active pixel sensors could be used, such as a two transistor, a four transistor, or a log scale implementation. As previously noted, some examples of general prior art design approaches to these other styles are shown in U.S. Patent Nos. 5,587,596; 5,926,214; and 5,933,190.

[0034] The present invention has thus been described in relation to a preferred and several alternate embodiments. One of ordinary skill after reading the foregoing specification will be able to affect various changes, alterations, and substitutions of equivalents without departing from the broad concepts disclosed. It is therefore intended that the scope of the letters patent granted hereon be limited only by the definitions contained in appended claims and equivalents thereof, and not by limitations of the embodiments described herein.

Claims

1. A photodiode formed in a semiconductor substrate of a first conductivity type, comprising:

   a first well of a second conductivity type formed in the semiconductor substrate;
   a first region of the first conductivity type with high concentration doping formed in the first well; and
   wherein the first region of the first conductivity type with the high concentration doping is not connected to the semiconductor substrate such that the first region is electronically floating.

2. The photodiode of Claim 1, wherein the semiconductor substrate is of the P type, the first well is of the N type, and the first region with the high concentration doping is P+, so as to form a P+/Nwell/Psub photodiode.

3. The photodiode of Claim 1, wherein the semiconductor substrate is of the N type, the first well is of the P type, and the first region with the high concentration doping is N+, so as to form an N+/Pwell/Nsub photodiode.

4. A pixel sensor formed in a semiconductor substrate having a first conductivity-type, said pixel sensor being for use in an imaging array, said pixel sensor having a photodiode comprising:

   a first well of a second conductivity type formed in the semiconductor substrate;
   a first region of the first conductivity type with high concentration doping formed in the first well; and
   wherein the first region of the first conductivity type with the high concentration doping is not connected to the semiconductor substrate such that the first region is electronically floating.

5. The pixel sensor of Claim 4, wherein the semiconductor substrate is of the P type, the first well is of the N type, and the first region with the high concentration doping is P+, so as to form a P+/Nwell/Psub photodiode.

6. The pixel sensor of Claim 4, wherein the semiconductor substrate is of the N type, the first well is of the P type, and the and first region with the high concentration doping is N+, so as to form a N+/Pwell/Nsub photodiode.

7. The pixel sensor of Claim 4, further comprising a second well of the first conductivity type formed in the semiconductor substrate next to the first well, the second well being formed either before or after

the first well.

8. The pixel sensor of Claim 7, further comprising:

a pair of field oxide regions on either side of the first and second wells, the field oxide regions being formed either before or after either or both of the first and second wells;
an isolation oxide layer over the wells; and
a gate over the second well.

9. The pixel sensor of Claim 8, further comprising second and third regions of the second conductivity type with high concentration doping, the second and third regions being under either side of the gate such that the second region is formed in the second well, and the third region is formed in parts of the first and second wells, the second and third regions being formed either before or after the first region.

10. The pixel sensor of Claim 9, wherein the second region is connected to a power supply voltage and the third region is connected to circuitry for reading out signals from the photodiode.

11. The pixel sensor of Claim 9, wherein the second well is of the P type, and the second and third regions with the high concentration doping are N+.

12. The pixel sensor of Claim 9, wherein the second well is of the N type, and the second and third regions with the high concentration doping are P+.

13. The pixel sensor of Claim 9, further comprising a fourth region of the second conductivity type, the fourth region being located beneath the first region and the third region, the fourth region being formed either before or after or in between the formation of the first region and the second and third regions.

14. The pixel sensor of Claim 9, wherein the field oxide region on the side of the first well further extends to at least partially cover the first region and the first well.

15. The pixel sensor of Claim 4, wherein the pixel sensor is formed in a passive pixel configuration.

16. The pixel sensor of Claim 4, wherein the pixel sensor is formed in an active pixel configuration.

17. The pixel sensor of Claim 4, wherein the pixel sensor is formed as a log scale cell.

18. The pixel sensor of Claim 4, wherein the pixel sensor is formed as a cell with two or more transistors.

19. The pixel sensor of Claim 18, wherein the cell has three transistors.

20. A pixel sensor cell comprising:

a photodiode with a P+/Nwell/Psub structure;
a reset transistor coupled to the photodiode for resetting the signal level on the photodiode;
a buffer transistor, the gate of the buffer transistor being coupled to the output of the photodiode; and
a row select transistor, the gate of the row select transistor being coupled to a row select signal line, the input of the row select transistor being coupled to the output of the buffer transistor, and the output of the row select transistor providing the output of the pixel sensor cell.

21. The pixel sensor cell of Claim 20, wherein the P+ region of the photodiode is electronically floating.

22. The pixel sensor cell of Claim 20, wherein the P+ region is formed as part of the PMOS source/drain implant that is done as part of the standard CMOS process such that the layout of the pixel sensor cell is fully compatible with the standard CMOS fabrication process.

23. The pixel sensor cell of Claim 20, further comprising a field oxide isolation layer over the edge of the photodiode.

24. The pixel sensor cell of Claim 23, wherein the field oxide isolation layer further extends over the P+ region and Nwell of the photodiode.

25. The pixel sensor cell of Claim 20, wherein the photodiode further comprises an additional N type region between the P+ region and the Nwell.

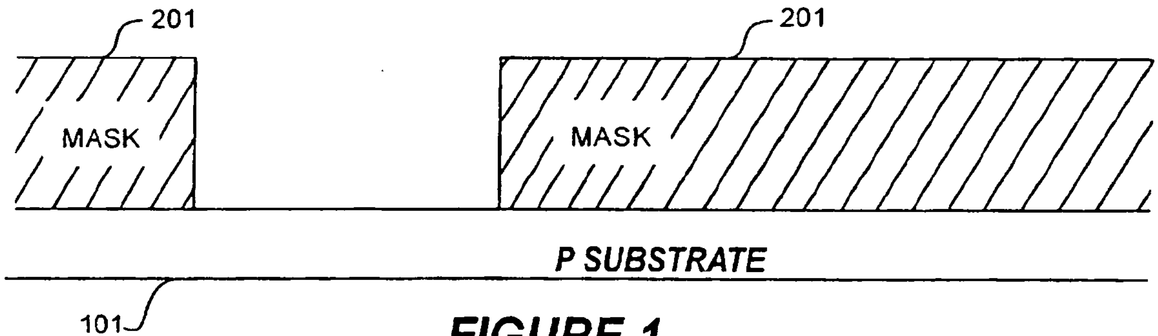

FIGURE 1

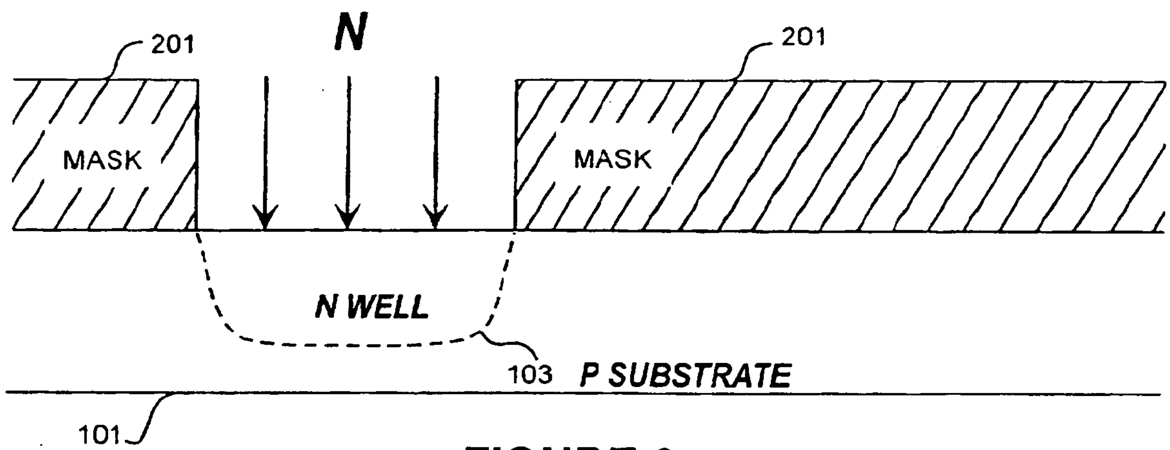

FIGURE 2

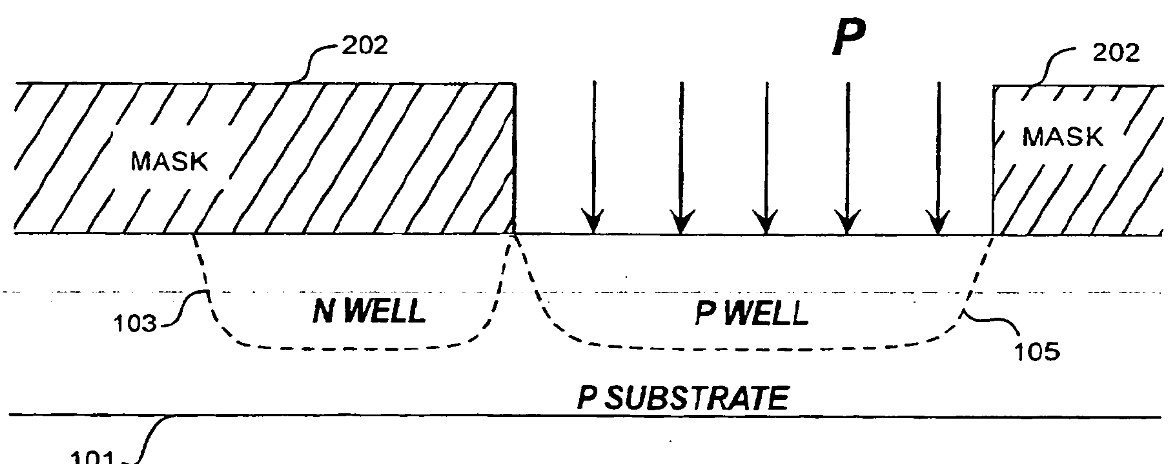

FIGURE 3

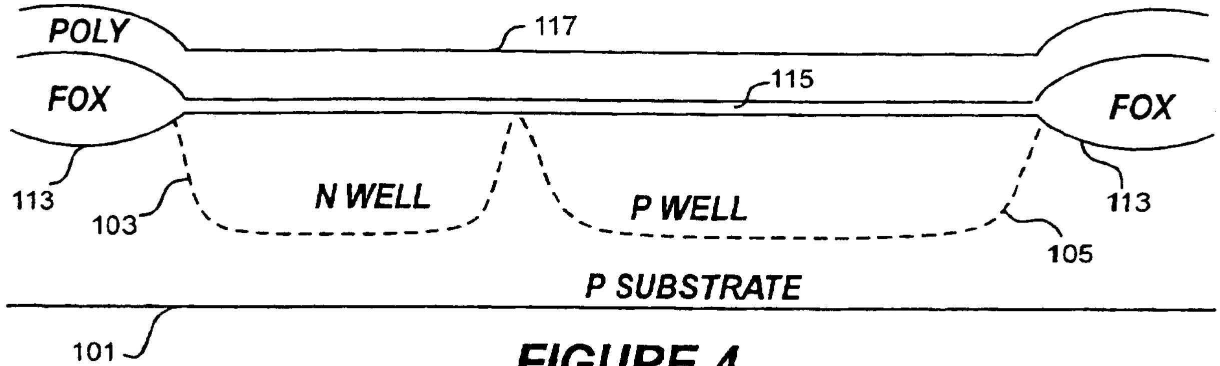

FIGURE 4

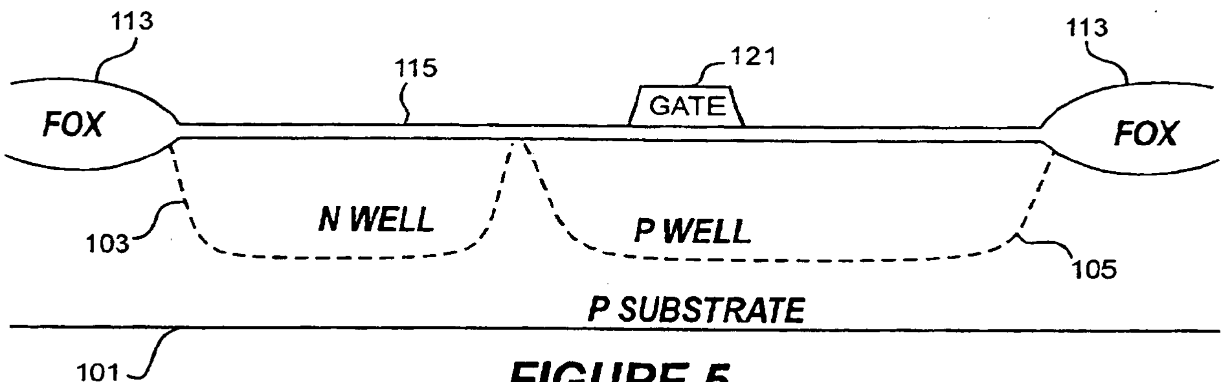

FIGURE 5

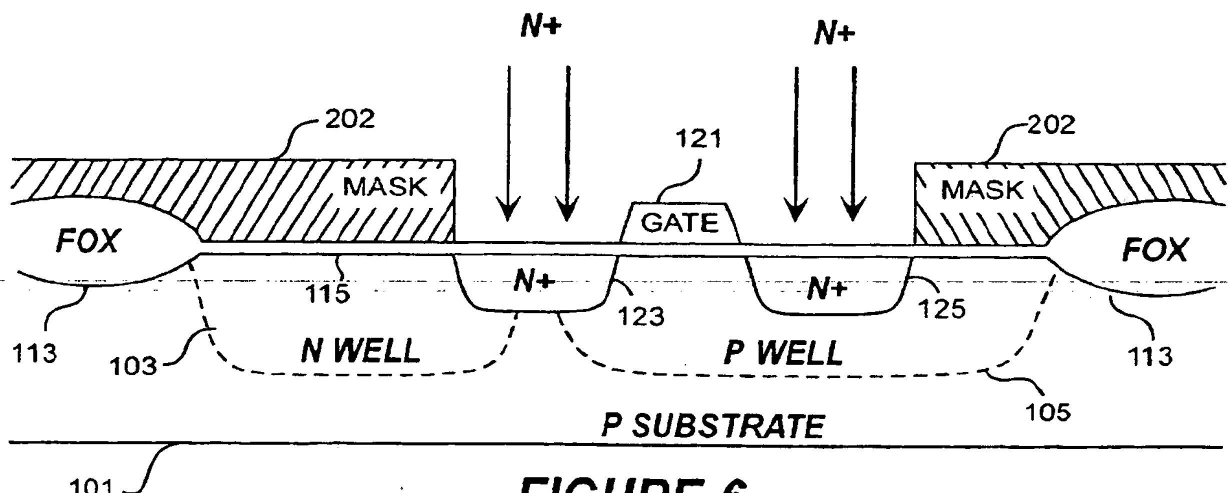

FIGURE 6

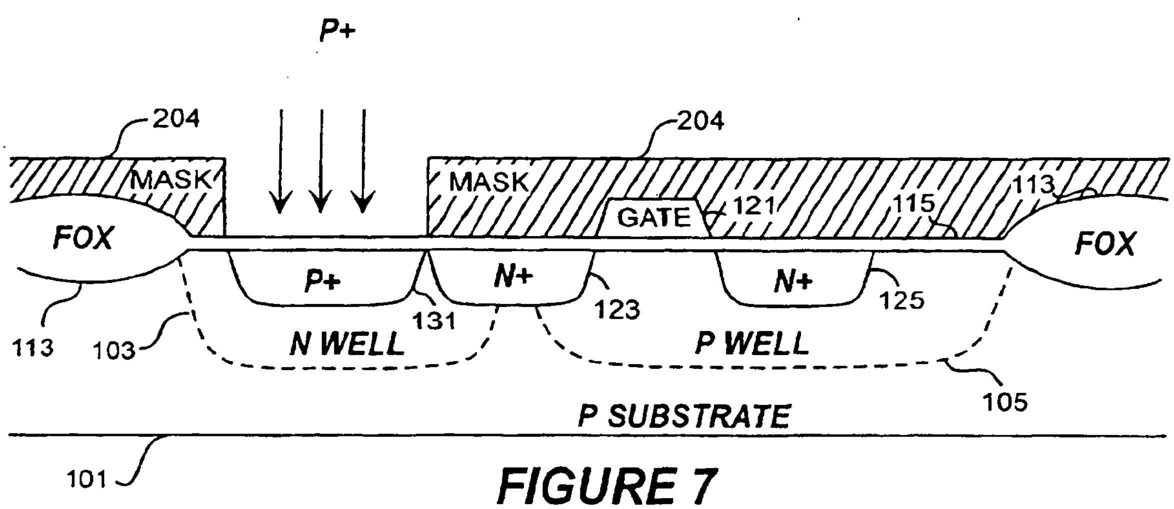

FIGURE 7

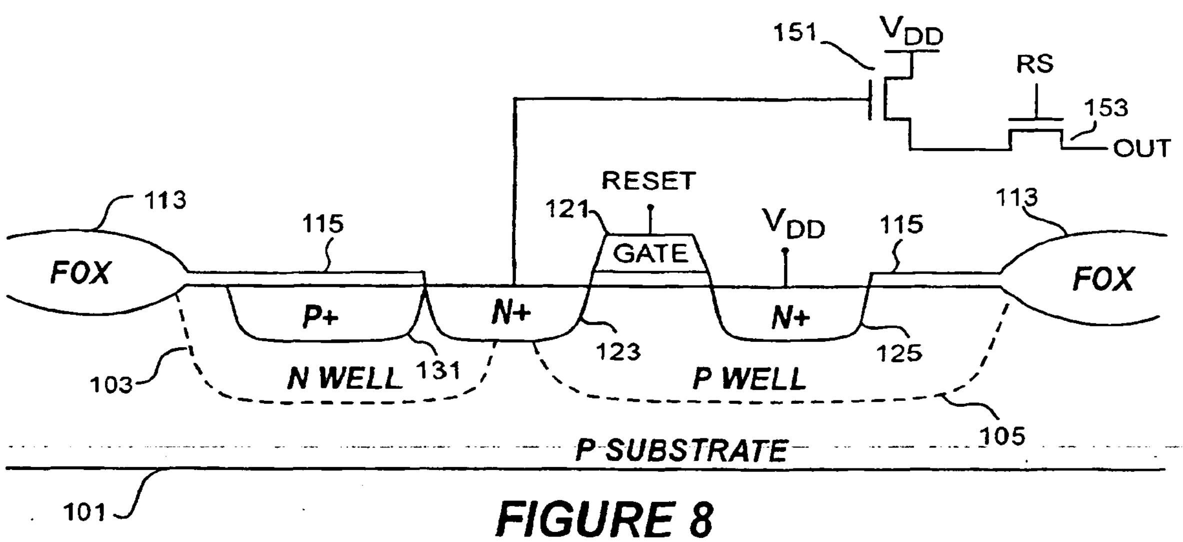

FIGURE 8

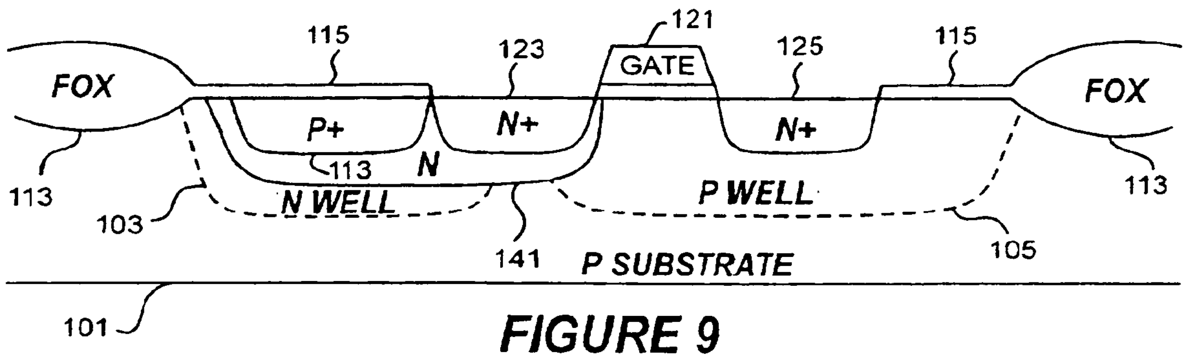

FIGURE 9

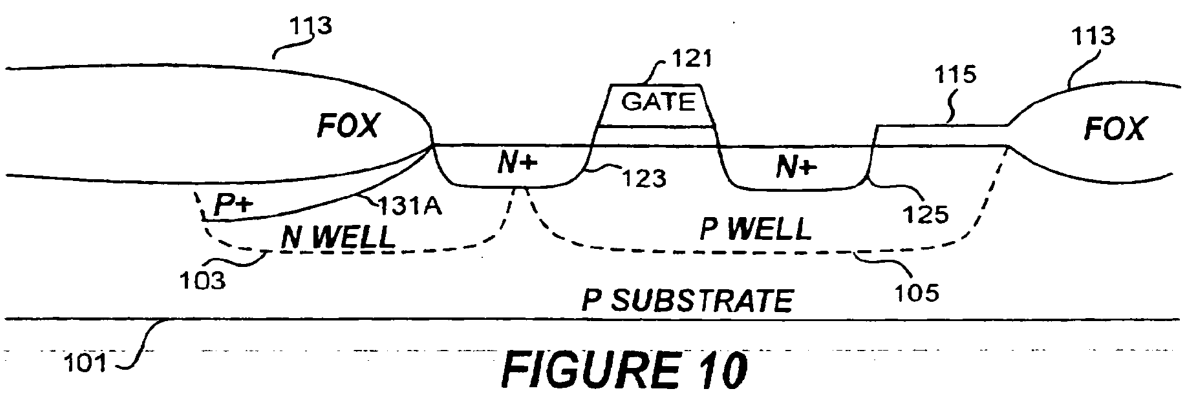

FIGURE 10